15. The integrated circuit of claim 14 including an inverter that creates a high signal in response to a low signal on said feedback path.

16. The integrated circuit of claim 15 including a pair of transistors that must both conduct in order to generate said pulses.

17. The integrated circuit of claim 16 including a capacitor circuit to enable the supply voltage to reach a designated output level.

18. The integrated circuit of claim 17 including a hysteresis sense stage coupled to said capacitor circuit.

19. The integrated circuit of claim 11 wherein said activation circuit includes an inverter coupled to the gate of a load transistor, a second transistor coupled to said load transistor and a third transistor coupled between said load transistor and said first transistor.

20. The integrated circuit of claim 11 including a circuit to latch the pulse generator in response to the supply voltage being in a first state.

21. A power-on reset pulse generator comprising:

a first circuit to develop a pulse indicating that a power supply voltage is not in a first state; and

a second circuit coupled to said first circuit to latch the first circuit in response to the power supply voltage being in the first state.

22. The generator of claim 21 wherein said second circuit latches the first circuit until the next power cycle.

23. The generator of claim 21 including a logic functionality that emulates logic that is difficult to trigger.

24. The generator of claim 23 wherein said logic functionality is coupled to the supply voltage.

25. The generator of claim 21 wherein said second circuit includes a level detector that detects when a voltage is above at least two transistor threshold voltages, said level detector operative to control said first circuit.

26. The generator of claim 21 including a feedback path from the output of said first circuit to said second circuit.

27. The generator of claim 26 including an inverter coupled in said feedback path.

28. The generator of claim 27 including a pair of transistors that must both conduct in order to generate said pulse.

29. The generator of claim 28 including a capacitor circuit to enable the supply voltage to reach a designated output level.

30. The generator of claim 29 including a hysteresis sense stage coupled to said capacitor circuit.